Approximating Complex Arithmetic Circuits with Formal Error Guarantees: 32-bit Multipliers Accomplished

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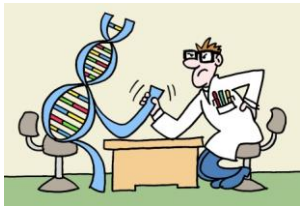
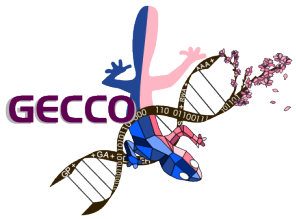




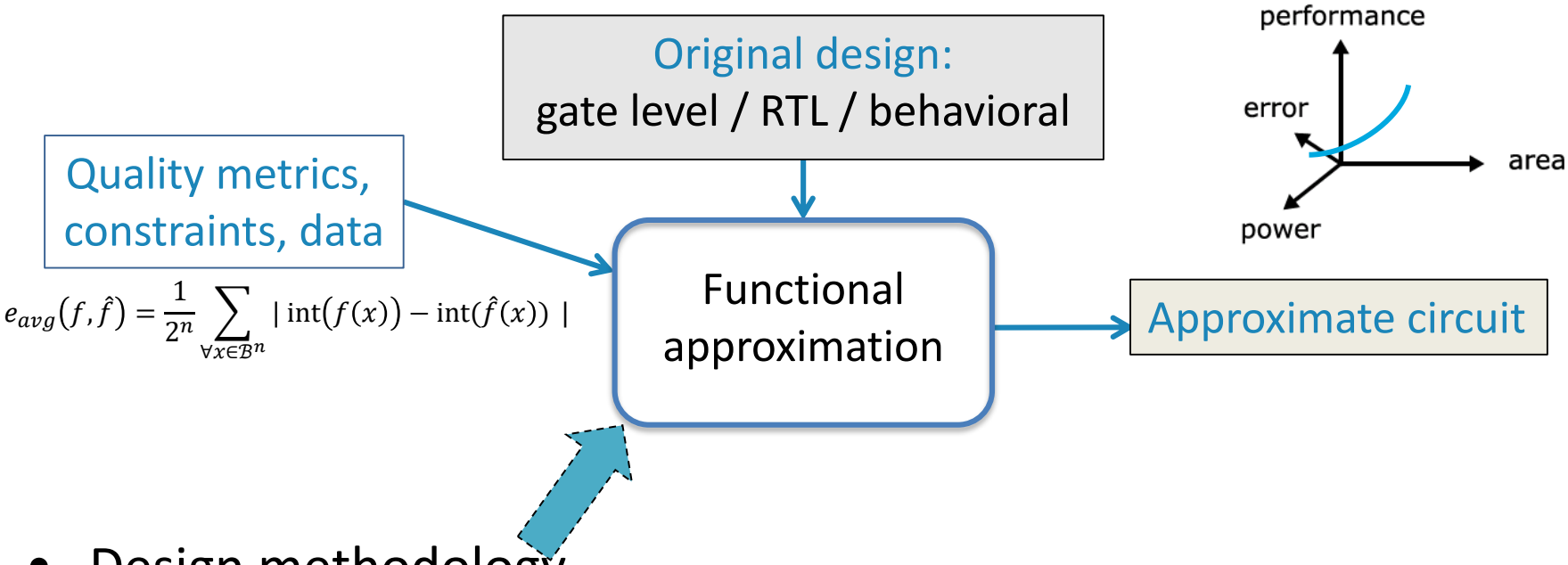
This entry is based on a paper:

- Milan Češka, Jiří Matyáš, Vojtěch Mrázek, Lukáš Sekanina, Zdeněk Vašíček, Tomáš Vojnar: **Approximating Complex Arithmetic Circuits with Formal Error Guarantees: 32-bit Multipliers Accomplished**. In: *Proceedings of 36th IEEE/ACM International Conference on Computer Aided Design* (ICCAD). Irvine, CA, IEEE, 2017, pp. 416-423.
  - ICCAD is a leading conference in electronic design automation, with the acceptance rate less than 25%, ranked “A” in CORE 2018 database.

Approximate computing

- Approximate computing addresses a radical shift from the `exact' computing paradigm, developed for dominant computer applications of previous decades, to **error-resilient and energy-efficiency driven computing**, which is typical for current deep neural networks, advanced image/video processing, big data, social network analysis, etc.
- "*The requirement of exact numerical or Boolean equivalence between the specification and implementation of a circuit is relaxed in order to achieve improvements in performance or energy efficiency.*" [Venkatesan et al., 2011]

Functional approximation of digital circuits



- Design methodology
  - Manual [Kulkarni et al.: J. Low Power Electronic 2011 and others]
  - Design automation methods (= some heuristics used)
    - SALSA (DAC 2012), SASIMI (DATE 2013), ABACUS (DATE 2014), ASLAN (DATE 2014), AIG-Rewriting (ICCAD 2016) …
    - Cartesian GP

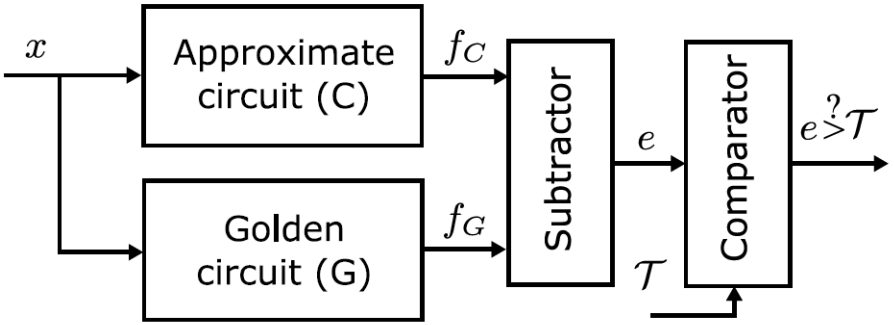
A complex multi-objective design/optimization problem!

Our contributions

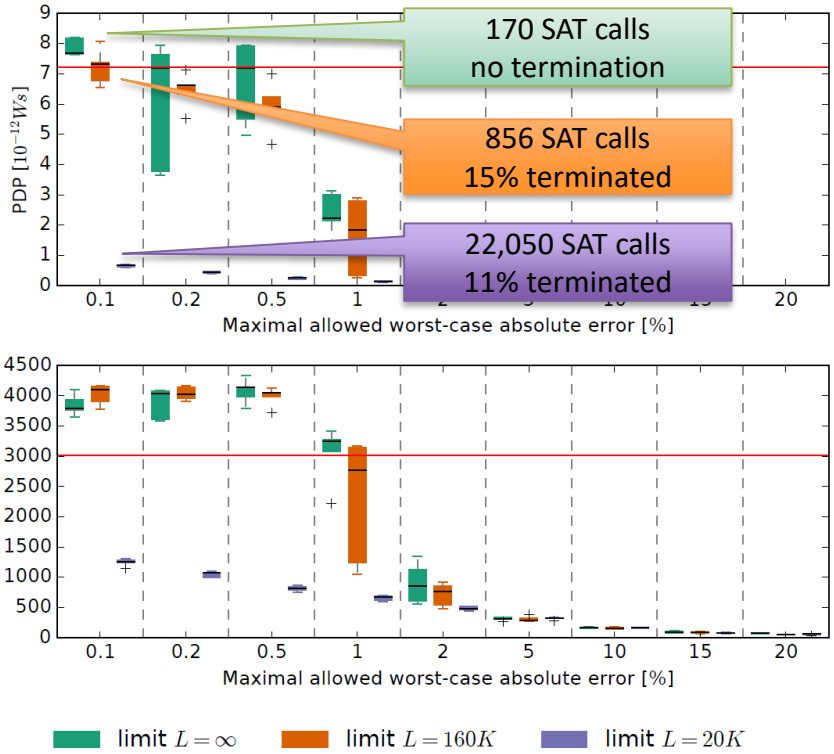
- CGP is used to approximate **complex** arithmetic circuits (such as 32 bit multipliers and 128-bit adders) in a fully automated multi-objective design scenario (with the error, power consumption and delay as the objectives).
- These circuits are approximated at the gate level **without introducing any decomposition** techniques.
  - All other approaches (including our approach from Humies 2015) need to introduce a decomposition strategy to approximate such complex designs!
- The **worst case absolute error** (WCAE) **is precisely evaluated** by means of a **SAT solving**-based technique for all candidate designs.
  - Other approaches only estimate the approximation error for complex circuits. The `exact' error is only computed for simple circuits such as 8-bit multipliers.
- Because our approach is search-based and fully automated, Pareto frontiers containing **many design alternatives are produced**
  - Other approaches typically produce only a few design alternatives.
- We introduced a **verifiability driven search** to discover high-quality approximate circuits.

The key innovation: Verifiability-driven search

- CGP is seeded with an ‘exact’ circuit.
- Worst case absolute error (WCAE) computation based on SAT solving.
- SAT solver is terminated if no decision is made after spending a predefined time => more candidate designs can thus be evaluated!
- CGP drives the search towards promptly verifiable approximate circuits showing a given WCAE!



$$fitness(C) = \begin{cases} size(C) & if\ WCAE(C) < \tau \\ \infty & else \end{cases}$$



- 16-bit multipliers for 9 target WCAE
- 2 hours/1 run
- 30 circuits analyzed for each WCAE
- Synopsys Design Compiler, 45 nm
- L is the max. number of conflicts for an AIG node, L = 160 K (~120 seconds) and L = 20 K (~3 seconds).

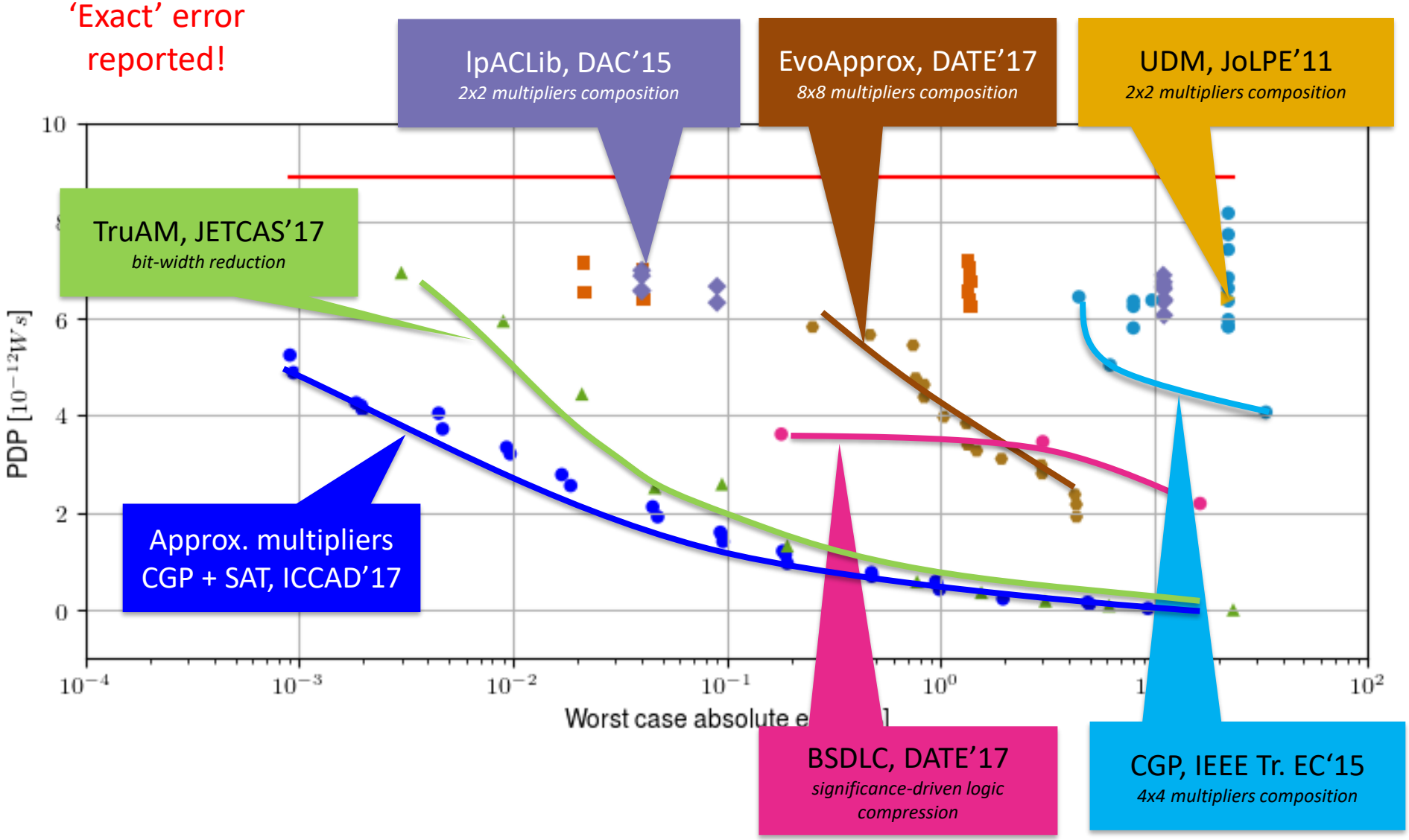
Why our result is “human-competitive”: **B**

- **B: “The result is equal to or better than a result that was accepted as a new scientific result at the time when it was published in a peer-reviewed scientific journal”**
- Journal papers [Jiang17, Vasicek15, Kulkarni11]) show tens of approximate 16 bit multipliers created by means of various techniques including evolutionary design. By means of the proposed method, we evolved multipliers showing better tradeoffs than existing multipliers as clearly demonstrated in the following figure.

- References:

  - [Jiang17] H. Jiang, C. Liu et al.: “A review, classification, and comparative evaluation of approximate arithmetic circuits,” J. Emerg. Technol. Comput. Syst., vol. 13, no. 4, pp. 60:1–60:34, Aug. 2017
  - [Kulkarni11] P. Kulkarni, P. Gupta, M. D. Ercegovac: Trading accuracy for power in a multiplier architecture. Journal of Low Power Electronics, vol. 7, no. 4, pp. 490–501, 2011. ISSN 1546-1998
  - [Vasicek15] Z. Vasicek, L. Sekanina: Evolutionary Approach to Approximate Digital Circuits Design. IEEE Transactions on Evolutionary Computation. 2015, vol. 19, no. 3, pp. 432-444

Comparison of selected 16-bit approximate multipliers



PDP is a Power Delay Product (Synopsys Design Compiler, 45 nm technological library)

Why our result is “human-competitive”: **D**

- We evolved (up to) 32 bit approximate multipliers and (up to) 128 bit approximate adders with formally guaranteed WCAE.
- In the case of multipliers, no approximate designs of this complexity are available in the literature for comparison.
- **D:** The evolved approximate multipliers presented in the paper are **publishable in their own right as a new scientific result - independent of the fact that they were mechanically created** - because no comparable designs exist in the literature. This is confirmed by the fact that our paper was accepted and presented at the prestigious ICCAD conference which (undoubtedly) has a high-quality review process.

Why our result is “human-competitive”: **E**

- E: **“Our result is equal to or better than the most recent human-created solution to a long-standing problem for which there has been a succession of increasingly better human-created solutions.”**
- This can be documented by a detailed comparison of the properties of evolved 16 bit approximate multipliers with the state of the art 16 bit approximate multipliers developed in recent years, which was conducted in the paper. The following table summarizes the human-created solutions.

Approximation strategies developed by human designers

Classification	Multiplier
Approximation in Generating partial products	Under-Designed Multiplier (UDM)
Approximation in the partial products	Broken Array Multiplier (BAM) Error Tolerant Multiplier (ETM) Approximate Wallace Tree Multiplier (AWTM) Truncated Wallace Multiplier (TruMW) Truncated Array Multiplier (TruMA)
Using approximate counters or compressors	Inaccurate Compressor based Multiplier (ICM) Approximate Compressor based Multiplier (ACM) Approximate Multiplier 1/2 (AM1/AM2) Truncated AM1/AM2 (TAM1/TAM2)
Approximate Booth multipliers	Fixed-width Booth multipliers

Han J.: Introduction to Approximate Computing, ESWEEK Tutorial 2017

Why our result is “human-competitive”: **G**

- G: **“proposed method solves a problem of indisputable difficulty in its field.”**
- Despite the fact that various design principles and methods for approximate arithmetic circuits were proposed in the last 8 year, the approximate circuit design problem is not solved and it is still considered as very hard. In particular, finding good compromises between key parameters of complex circuits such as 16 or 32 bit multipliers is very difficult. We presented better solutions than the state of the art.

5 reasons why we should win a prize

1. We contributed to solving one of the key challenges discussed globally – how to reduce energy requirements of current society.
2. By means of CGP we created much better approximate multipliers and adders than the state of the art methods can create.
   - Moreover, formal guarantees in terms of the approximation error are provided by our method.
3. We invented a new and highly efficient evolutionary circuit design method that drives the search towards promptly verifiable approximate circuits.

5 reasons we should win a prize

4. We influenced several research communities (outside the EA):
   - Our result was well-accepted on a leading electronic CAD conference – ICCAD 2017.
   - Our result was later presented as a key idea behind a tool paper accepted on the flagship formal verification conference (CAV 2018, A* according to CORE database).
     - Milan Češka, Jiří Matyáš, Vojtěch Mrázek, Lukáš Sekanina, Zdeněk Vašíček, Tomáš Vojnar: In: ADAC: Automated Design of Approximate Circuits. Proceedings of 30th International Conference on Computer Aided Verification (CAV'18), LNCS, to appear, 2018, pp. 1-9
5. Evolved approximate arithmetic circuits are now available online, in the EvoApprox library
   http://www.fit.vutbr.cz/research/groups/ehw/approxlib/
   - 134 unique users from 23 countries visited the library website and spent there approximately 4 minutes on average in last 3 months.

Thank you!