Analog Integrated Circuits and Signal Processing, 40, 83–85, 2004

Novel Canonic Current Mode DDCC Based SRCO Synthesized Using a Genetic Algorithm

VARUN AGGARWAL

Division of Electronics and Communication, Netaji Subhas Institute of Technology, New Delhi 110045, India
E-mail: varun.aggarwal@vsnl.net

Received June 24, 2003; Revised July 24, 2003; Accepted July 30, 2003

Abstract. A survey of the technical literature reveals that synthesis of Current Mode (CM) oscillators using single active building block (ABB) requires an additional identical or complementary current terminal to sense and take out the current output. The topologies of these oscillators are essentially based on the current mode approach. They use a Voltage Controlled Voltage Source (VCVS) and two current terminals to implement the CM oscillator. In the present paper, a novel DDCC (Differential Difference Current Conveyor, introduced in Chiu et al. (*IEE Proc., Circuits, Devices, Syst.,* vol. 143, no. 2, pp. 91–96, 1996)) based canonic CM Single-Resistor Controlled Oscillator (SRCO) is presented, which uses a VCVS and a single current terminal to take out the output. Earlier, authors used DDCCC (Differential Difference Complementary Current conveyor), DVCCC (Differential Voltage Complementary Current Conveyor) to implement CM oscillators and hypothesized the requirement of an additional current terminal for the output. The synthesis of present topology indicates that DDCC is a versatile building block to implement canonic CM SRCOs and doesn't need any additional current terminal. This topology was synthesized using an innovative genetic algorithm. Spice simulations have been included and they verify theoretical results.

Key Words: oscillators, current conveyors, genetic algorithm

Introduction

Current mode (CM) sinusoidal oscillators using minimum components have been of interest with the recent popularity of the current mode approach of IC design. Some topologies of CM oscillators using a single ABB have been proposed earlier [1–3]. A review of these topologies reveal that these circuits use an additional identical or complementary current terminal (for taking out the quadrature current output) apart from the one being used as a part of the oscillator topology. These topologies are essentially based on the current mode approach. They use a single VCVS or buffer and two additional current terminals. One of these terminals is a part of the topology, while the other is used to sense the output current. Only the topologies suggested in [2] implements an oscillator using OMA (Operational Mirrored Amplifier), where the topologies proposed are voltage mode topologies and the current output is drawn from the complementary output of the OMA. However, these topologies are not canonic and require six and seven passive elements for Single Frequency Oscillators (SFOs) and SRCOs respectively.

Similarly, authors hypothesized that an additional current terminal would be needed to implement CM SRCOs using DVCC (introduced in [8], already has two current terminal) and DDCC. Therefore, existing topologies use DDCCC [4] and DVCCC [3] for implementation of CM oscillators. In this letter, we present a single DDCC based CM SRCO, which essentially has a voltage mode topology and doesn't need any extra current terminal. The circuit topology uses a single VCVS ($v_x = v_{y1} - v_{y2} + v_{y3}$, characteristic of DDCC) to implement the oscillator topology and the single available current terminal to provide the output current. The oscillator is canonic, i.e. it uses only five elements and a single DDCC [5]. The topology not only fills the void discussed above, but is also important in view of the fact that application of a DDCC to implement a CM SRCO has not been discussed till date. This topology was synthesized using an innovative genetic algorithm [6].

Genetic Algorithm to Synthesize Oscillators

A versatile genetic algorithm [6] has been developed which can be used to synthesize topologies of sinusoidal oscillators using different ABBs. The algorithm searches for topologies of a sinusoidal oscillator using a given ABB and finally presents the topology and characteristic equation of the oscillator in terms of resistor and capacitor values. As a case study, the algorithm was able to generate all the twelve canonic opamp-based SFOs proposed in [7]. However, the algorithm is incapable of ascertaining whether the complete set of topologies has been found. Some interesting three capacitor opamp based oscillators were also generated. The algorithm was also used to generate topologies using OTRA (Operational Trans-Resistance Amplifier) and presently experiments are being conducted to synthesize DVCC, DDCC, DDCCC based topologies and also grounded capacitor oscillators. The final aim of the algorithm is to fully automate the synthesis and study of sinusoidal oscillators.[1]

Proposed Topology

The proposed canonic DDCC based CM SRCO is shown in Fig. 1. DDCC has the following characterizing equations:

$$i_{y1} = i_{y2} = i_{y3} = 0$$
$$v_x = v_{y1} - v_{y2} + v_{y3}$$
$$i_z = i_x$$

Routine analysis yields the Condition of Oscillation (CO) and Frequency of Oscillation (FO) as

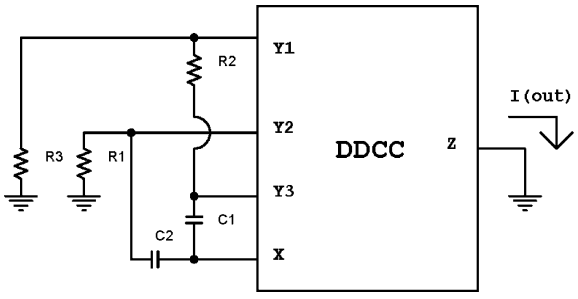

Fig. 1. Proposed DDCC based canonic CM SRCO.

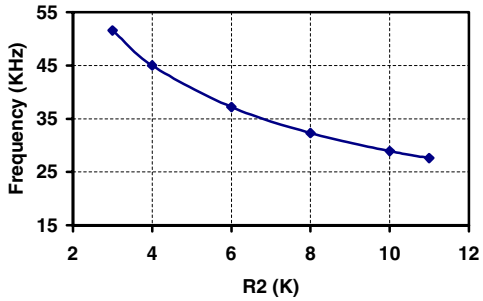

Fig. 2. PSPICE simulation results: Variation of FO with R_2.

follows:

$$\text{CO} : 2C_2R_1 - C_1R_3 = 0 \tag{1}$$
$$\text{FO} : f_o = \frac{1}{2\pi\sqrt{C_1C_2R_1R_2}} \tag{2}$$

The FO and CO are independently controllable by R_2 and R_3 respectively. The output current I(out) is available from Z.

Simulation Results

The PSPICE simulations were performed using a CMOS realization of DDCC as in [4] (using 1.20 μ, level 3 MOSFET parameters obtained through MOSIS). The aspect ratio, biasing current and supply voltages were chosen as in [8]. The circuit was designed with the following parameter values: $C_1 = C_2 = 1$ nF, $R_1 = 3$ KΩ, $R_3 = 6$ KΩ, $R_2 = 3$–11 KΩ. The variation of FO with R_2 is shown in Fig. 2. The circuit behaved satisfactorily over the given range. It showed some negative clipping beyond the range, which is probably a limitation of DDCC implementation used.

Conclusion

A new canonic CM DDCC based oscillator has been proposed. It is the only canonic CM SRCO, which has a voltage mode topology and uses a single current output. It is shown that DDCC is a versatile ABB to implement such oscillators. The oscillator has simple CO and FO, which are non-interactively controllable. The feasibility of the circuit has been confirmed by PSPICE simulations. A catalogue of minimum component CM oscillators using single DDCC and DDCCC synthesized by the genetic algorithm [6] is

being developed and shall be submitted for publication shortly.

Acknowledgment

I will like to thank Prof. Uğur Çam, Dokuz Eylül University, Izmir, Turkey and Prof. Raj Senani, AIC Lab, NSIT, Delhi for their academic help and guidance.

Note

1. More information regarding the algorithm is available from the author on request.

References

1. S. Celma and P.A. Martinez, "Transformation of sinusoidal RC oscillators using universal active elements." *IEE Proc. Circuits, Devices, Syst.*, vol. 142, no. 6, pp. 353–356, 1995.
2. R. Senani, "On the equivalent forms of single op-amp sinusoidal oscillators." *IEEE Trans. Circuits Syst. I*, vol. 41, no. 10, pp. 617–624, 1994.
3. S.S. Gupta and R. Senani, "Grounded-capacitor current mode SRCO, novel application of DVCCC." *Electron. Lett.*, vol. 36, no. 3, pp 195–196, 2000.
4. S.S. Gupta and R. Senani, "Comment, CMOS differential difference current conveyors and their applications." *IEE Proc., Circuits, Devices, Syst.*, vol. 148, no. 6, pp. 335–336, 2001.
5. W. Chiu, S.I. Liu, H.W. Tsao, and J.J. Chen, "CMOS differential difference current conveyors and their applications." *IEE Proc., Circuits, Devices, Syst.*, vol. 143, no. 2, pp. 91–96, 1996.
6. V. Aggarwal, "Evolving sinusoidal oscillators using genetic algorithms," in *Proc., The 2003 NASA/DoD Conference on Evolvable Hardware*, Chicago, USA, 2003, pp. 67–76.
7. B.B. Bhattacharya and M. Darkani, "A unified approach to realization of canonic RC-active, single as well as variable frequency oscillators using operational amplifier." *Journal of Franklin Inst. (Germany)*, vol. 317, no. 6, pp. 413–419, 1984.
8. H.O. Elvan and A.M. Soliman, "Novel CMOS differential voltage current conveyor and its applications." *IEE Proc. Circuits Devices Syst.*, vol. 144, no. 3, pp. 195–200, 1997.